Graphene Semiconductor Field Effect Transistor

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Introduction

•Microelectronic industry has scaled the transistor feature size from 10µm in 1975 to almost 22nm in 2014 to improvise on cost, performance and power consumption.

•As the scaling continues, a material compatible with the sub-10nm regime would be of great interest that can preserve the MOSFET principles giving better performance.

•Graphene and Graphene oxide being compatible with each other can foresee transistor devices of the smallest possible dimensions.

Background

The semiconductor industry scaled down feature size over the years through the following technologies [2]:

❖ Bulk type-A technology in which the source and drain terminals are diffused inside the bulk with an ideal gate contact separated by a dielectric material.
❖ SOI (Silicon On Insulator)- Use of a layered silicon–insulator–silicon substrate in place of a conventional silicon substrate to improve the performance.
❖ FinFET - The conducting channel is wrapped by a thin silicon **fin** forming the body of the device with the thickness defining the effective channel length of the device.

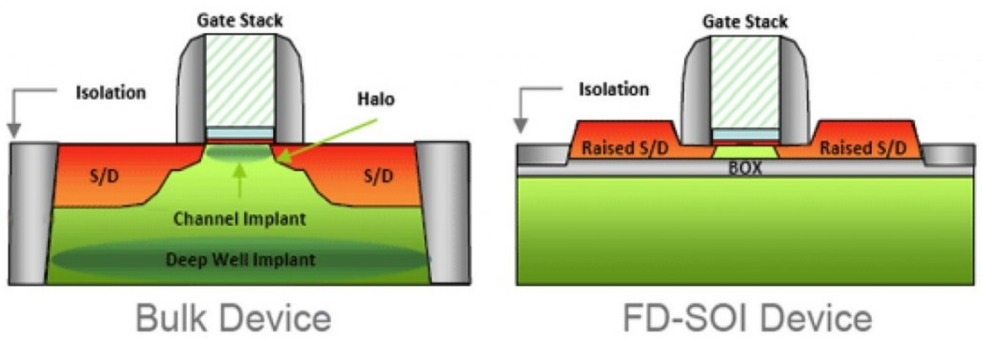

Figure 1: Bulk ,SOI and FinFET layout

Results

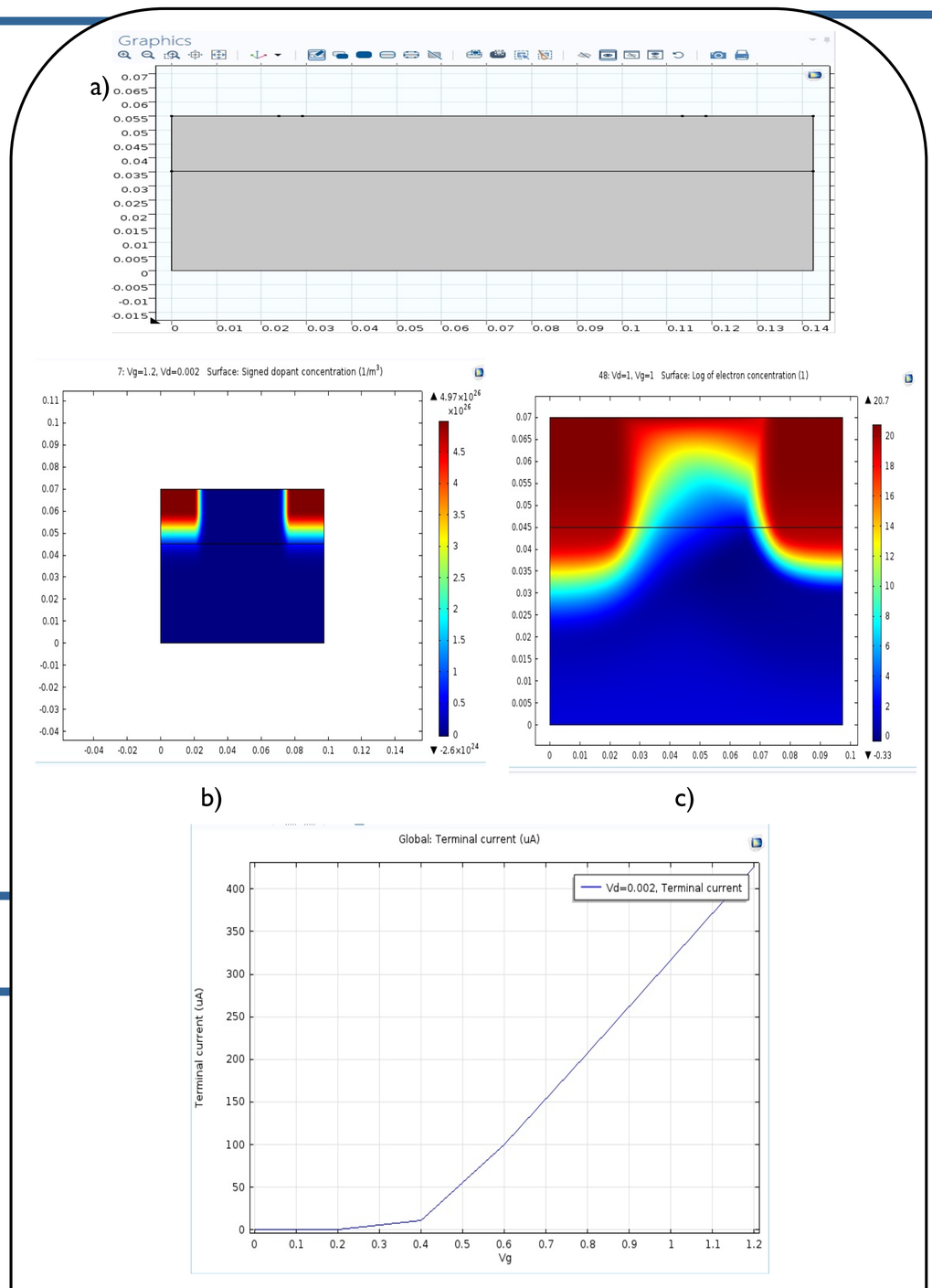

Figure 2: 65nm technology node a)layout; b)doping level; c)Electron concentration; d)DC characteristics – V_{gs} VS I_d

Methods

- Simulation of graphene based transistor is performed using COMSOL Multiphysics software (semiconductor module) in which modeling of a 2D MOSFET device is used.
- The solution for the transistor DC characteristics, turn-on voltage, concentrations of electrons and holes and doping profiles.
- Finite element method was utilized for the physical calculations in correspondence with the initial and boundary conditions.

Discussion

The boundary conditions for the layout are from PTM(Predictive Technology Models) and the effective gate length of the channel is calculated as

$$L_{eff} = L_{drawn} - 2l_{int}$$

However after 2006 with further scaling of transistor sizes, the formula was modified taking into account the proximity effect for the lithography process, the equation now being:

$$L_{eff} = L_{drawn} + x_l - 2l_{int}$$

x_l – proximity length parameter

Conclusion and further research

The simulation study performed gives us a positive result with the electrical characteristics, giving us a future goal to improvise transistor devices with graphene and graphene oxide [1] materials using FD-SOI as well as FinFET technologies.

References

[1]. Lemme, M. C., Echtermeyer, T. J., Baus, M., Szafranek, B. N., Bolten, J., Schmidt, M., . . . Kurz, H. (2008). Mobility in graphene double gate field effect transistors. Solid-State Electronics, 52(4), 514-518.
[2]. Yan, R. H., Ourmazd, A., & Lee, K. F. (1992). Scaling the Si MOSFET: from bulk to SOI to bulk. IEEE Transactions on Electron Devices, 39(7), 1704-1710. doi: 10.1109/16.141237